

VERTICAL COMPOUND SEMICONDUCTOR FIELD EFFECT
TRANSISTOR STRUCTURE

5

Related Applications

- [0001]** This application is related to co-pending U.S. patent application 10/_____, Attorney Docket No. ONS00502, entitled "DC/DC CONVERTER WITH DEPLETION MODE COMPOUND SEMICONDUCTOR FIELD EFFECT TRANSISTOR SWITCHING DEVICE", by Peyman Hadizad, assigned to the same assignee, Semiconductor Components Industries, LLC, filed concurrently herewith, and which is incorporated by reference for all purposes.
- [0002]** This application is further related to co-pending U.S. patent application 10/_____, Attorney Docket No. ONS00505, entitled "METHOD OF MAKING A VERTICAL COMPOUND SEMICONDUCTOR FIELD EFFECT TRANSISTOR DEVICE", by Peyman Hadizad, assigned to the same assignee, Semiconductor Components Industries, LLC, filed concurrently herewith, and which is incorporated by reference for all purposes.

25

Background of the Invention

- [0003]** This invention relates generally to high frequency power semiconductors, and more specifically to compound semiconductor field effect transistor (FET) structures and applications thereof.
- [0004]** In the area of computer and peripheral power supply applications, there are several factors driving future performance and demand. Such factors include an increase in output power requirements because of higher microprocessor speeds, smaller system size (i.e., reduced circuit board space), lower cost, improved transient response, and lower output voltage ripple (i.e., lower microprocessor operating voltages). Additionally, advancing microprocessor needs, which include decreasing

operating voltage and increasing current requirements, will require power conversion devices and circuits that enable highly efficient and tightly regulated power.

These devices and circuits must operate at higher

5 frequencies and exhibit enhanced thermal characteristics.

[0005] Electronic systems such as computer and peripheral power supply applications often require that multiple dc voltage levels be produced from a single dc voltage source. This conversion is done with electronic
10 circuits such as dc/dc converters. A basic converter circuit is a two-port network having a pair of input terminals and a pair of output terminals. A dc power source is coupled across the two input terminals, and a dc load is coupled across the two output terminals.

15 Within the two-port network, the circuit typically comprises multiple switching devices, appropriate control circuitry, one or more capacitors, and one or more inductors. Typical dc/dc converters include the buck converter, the boost converter, and the buck-boost
20 converter.

[0006] An ideal switching device has two states: on and off. In the on state, the ideal device conducts current between two terminals with zero voltage drop across the terminals. In the off state, the ideal device
25 will support any voltage drop across the terminals while conducting zero current between them. A number of different semiconductor devices are used as switches in dc/dc converters, all of which depart from the ideal switching device in one or more ways. Examples of such
30 devices include diodes, bipolar transistors, MOSFETs, silicon controlled rectifiers, and junction field effect transistors.

[0007] One problem with typical switching devices is a non-zero voltage between the terminals when in the on
35 state. This results in power dissipation in the switching device, which generates heat and reduces

overall circuit efficiency. A second problem involves the dynamic characteristics of the switching device when transitioning between the on state and the off state. Slow switching speeds place a limit on system operating frequency and duty cycle. Each time a device switches between states, a certain amount of energy is lost. The slower a device switches, the greater the energy lost in the circuit. This has significant impact on high frequency and/or high power applications, and contributes significantly to the reduction of overall efficiency of a dc/dc converter.

[0008] Most losses in switching power circuits are determined by the physical properties of semiconductor devices. Although silicon based MOSFET devices are a primary choice for many power conversion applications, they have inherent limitations for high frequency applications due to their physical structure. Such limitations include high reverse recovery charge, high gate charge, and high on resistance, which detrimentally impact power dissipation and thermal response characteristics.

[0009] Multi-phase dc/dc conversion is a preferred technique for addressing the high current/low operating voltage requirements of present and future microprocessors. In multiphase dc/dc converter architectures, a load is distributed evenly across phase-shifted pulse-width-modulation (PWM) channels and associated switching devices and inductors. This approach spreads power and current dissipation across several power handling devices thereby lowering stress on components. This approach also reduces output ripple on inductor current.

[0010] By way of example, a typical silicon-based multi-phase dc/dc converter for a 120 Amp, 500 kHz microprocessor system consists of four phases. A silicon-based multi-phase dc/dc converter for 1 MHz/120

Amp microprocessor system may consist of five phases, and a silicon-based multi-phase dc/dc converter for a 2 MHz/120 Amp system may consist of seven phases.

5 [0011] In multi-phase dc/dc converters, current levels are often sensed in each phase as a means of feedback control within a system. This is done typically using on-resistance of a silicon switching MOSFET device or series resistance of an output inductor. The on-resistance method current sensing is problematic due to
10 variations in processing for silicon MOSFETs devices, which becomes even more of a problem at higher current levels. Additionally, with improvements in inductor designs and fabrication methods, the series resistance current sensing technique has become less reliable
15 because the improvements make it difficult to distinguish the inductor resistance from system noise.

[0012] Accordingly, a need exists for switching devices suitable for the increasingly stringent demands of applications such as dc power conversion.
20 Additionally, it would be beneficial for such devices to make possible accurate phase current sensing.

Brief Description of the Drawings

25 [0013] FIG. 1 illustrates, an enlarged cross-sectional view of a portion of a vertical FET device according to the present invention;

[0014] FIG. 2 illustrates a partial top plan view of a
30 gate control structure for device of FIG. 1;

[0015] FIG. 3 illustrates an enlarged cross-sectional view of a portion of an edge termination structure for the device of FIG. 1;

[0016] FIG. 4 illustrates a circuit diagram including
35 the device of FIG. 1 together with a sense FET device according to the present invention;

[0017] FIG. 5 illustrates a simplified top plan view of embodiment of FIG. 4; and

[0018] FIG. 6 illustrates an enlarged cross-sectional view of a portion of the embodiment of FIG. 4.

5

Detailed Description of the Drawings

[0019] In general, the present invention pertains to a vertical compound semiconductor junction field effect transistor (JFET) structure. In a preferred embodiment, a first trench is formed in an upper surface of an n-type conductivity compound semiconductor layer, and a second trench is formed within the first trench to form a gate region. The gate region is then doped by ion implanting a p-type dopant species such as Be^+ into the lower sidewalls and bottom surface of the second trench. N-type source regions are formed on both sides of the double trench gate region. The opposite surface of the n-type conductivity compound semiconductor layer provides a drain region. The doped gate region extends along the channel region and is separated from the source regions to provide, among other things, an improved gate blocking characteristic. A gate-coupling region is used to connect a plurality of closely spaced doped gate regions. In a preferred embodiment, the structure comprises an n-channel depletion mode GaAs FET.

[0020] Unlike silicon, GaAs is a direct bandgap compound semiconductor material with an inherent property of high electron mobility ($8500 \text{ cm}^2/\text{V}\cdot\text{sec}$), which is greater than 4X that of silicon ($1500 \text{ cm}^2/\text{V}\cdot\text{sec}$). Also, GaAs has a larger bandgap of 1.42 eV compared to 1.1 eV for silicon, which provides, among other things, enhanced performance at elevated temperatures. Additionally, the reverse recovery charge of a GaAs FET device is approximately 100X lower than that of a silicon FET device. The double trench gate design according to the

35

present invention together with a compound semiconductor material provides a vertical FET structure with improved switching and on resistance characteristics compared to silicon switching devices.

5 **[0021]** The present invention is better understood by referring to FIGS. 1-6 together with the following detailed description. For ease of understanding, like elements or regions are labeled the same throughout the detailed description and FIGURES where appropriate.

10 Although the embodiment shown and described is a depletion mode n-channel FET device, the structure according to the present invention is suitable for p-channel and enhancement mode devices as well.

15 **[0022]** FIG. 1 shows an enlarged cross-sectional view of a vertical FET device or compound semiconductor vertical FET or JFET structure 11. Structure 11 comprises a body of semiconductor material 13, which preferably includes a starting or supporting substrate or wafer 14 having an upper surface 16. An epitaxial or drift layer or layers 17 is formed on upper surface 16. Body of semiconductor material 13 includes an upper or source surface 19 and a lower or opposing surface 21. Preferably, body of semiconductor material 13 comprises a compound semiconductor such as GaAs, InP or the like.

20 Although only a portion of a FET device or cell is shown, structure 11 comprises a plurality of individual vertical FET devices or cells connected in parallel. Structure 11 forms, for example, a power switching FET or a sense FET.

25 **[0023]** In a preferred embodiment for an n-channel depletion mode (i.e., normally on) device, substrate 14 comprises n-type GaAs, and layer 17 comprises an n-type GaAs epitaxial layer, which preferably has a lower dopant concentration than substrate 14. The thickness and dopant concentration of layer 17 varies as a function of

30 the desired device characteristics. Preferably, for a depletion mode FET device, layer 17 has a dopant

concentration on the order of less than 5×10^{17} atoms/cm³ and a thickness greater than about 0.1 microns. Layer 17 is formed using conventional compound semiconductor epitaxial growth methods. The dopant profile of layer 17 is substantially constant, or the profile is graded depending on desired device characteristics. Alternatively, body of semiconductor material 13 comprises InP.

[0024] Source regions 26 are formed in and extend from upper surface 19. When layer 17 comprises an n type material, source regions 26 comprise n⁺ regions and preferably are formed using ion implantation techniques. For example, source regions 26 are formed using Si⁺ implantation at a dose sufficient to lower contact resistance to subsequently formed contact layers. For example, a Si⁺ dose of about 4.0×10^{13} atoms/cm² with an implant energy on the order of 85 KeV being typical. Alternatively, selenium, tin, or tellurium is used to form source regions 26. In an alternative embodiment, multiple source implants at different implant doses and implant energies are used.

[0025] Structure 11 further includes a double trench gate, double groove gate, multiple trench gate, trench within a trench gate, or stepped trench gate structure 28 formed in and extending from upper surface 19 into layer 17. Preferably, trench structure 28 includes a first trench or groove portion 29 having a width 31 in a range from about 0.3 microns to about 1.5 microns, and a depth 32 in a range from about 0.5 microns to about 5 microns.

[0026] Trench structure 28 further includes a second trench or groove portion 34 having a width 36 in a range from about 0.25 microns to about 1.4 microns, and a depth 37 in a range from about 0.5 microns to about 5 microns. Preferably, the pitch or centerline-to-centerline distance 41 of adjacent trench gate structures 28 is in a range from about 1.3 to about 4.5 microns. These

dimensions are variable according to specific device requirements. That portion of layer 17 between gate structures 28 forms channels or channel regions 61.

5 **[0027]** Structure 11 also includes doped gate regions 59, which preferably extend along sidewalls and lower surfaces of second trenches 34. For an n-channel device, doped gate regions 59 are p-type, and are formed preferably using angled ion implantation. Preferably, gate regions 59 and source regions 26 are activated using
10 rapid thermal processing with a temperature up to about 900°C for about 10 to 30 seconds being sufficient.

15 **[0028]** Trench structures 28 preferably are formed using reactive ion etching (RIE) or damage free electron cyclotron resonance (ECR) etching, which provides clean and straight sidewall features. A chlorine-based etch chemistry is preferred. In a preferred embodiment, second trench 34 is formed using spacers formed on the
sidewalls of first trench 29, which are subsequently removed.

20 **[0029]** A dielectric or passivation layer 63 is formed over upper surface 19 including trench structures 28. Preferably, passivation layer 63 comprises a silicon nitride with a thickness in a range from about 0.05 microns to about 0.3 microns. Preferably, plasma
25 enhanced chemical vapor deposition (PECVD) is used to form passivation layer 63. A dielectric layer is then formed over passivation layer 63, and planarized to form a trench-fill layer 66. Trench-fill layer 66 provides for, among other things, better step coverage for
30 subsequently formed conductive layers, and preferably comprises a low temperature oxide, silicon nitride, or a spin on dielectric. Trench-fill layer 66 is formed using etch-back or chemical mechanical planarization (CMP) techniques.

35 **[0030]** Openings are then formed in dielectric layer 63 to provide contacts to source regions 26. Additionally,

portions of trench-fill layer 66 and passivation layer 63 are removed to expose portions of a gate connecting region 79 (shown in FIG. 2). A first metal or contact layer formed over upper surface 19, and patterned to provide a source contact 84 and a gate contact 86 (shown in FIG. 2). Source contact layer 84 and gate contact layer 86 preferably comprise NiGeAu, NiGeW, or other suitable metal. A second contact layer or metal layer 87 is formed over source contact 84 and gate contact 86. Second metal layer 87 preferably comprises nickel or gold, and is formed using electroplating or electroless plating techniques. Body of semiconductor material 13 is thinned using a backgrind step, and a back metal or drain contact layer 88 is deposited on lower surface 21. Drain contact layer 88 comprises NiGeAu, or another suitable metal.

[0031] FIG. 2 shows an enlarged partial top plan view of a preferred gate contact structure 71, which includes doped connecting region 79. Doped gate connecting region 79 ties or couples together a plurality of doped gate regions 59 in a single contact region. For ease of understanding, structure 11 shown in FIG. 1 is taken along reference line 1-1 of FIG. 2. Phantom line 89 represents an alternative placement for gate contact layer 86. Doped termination region 159 and termination contact layer 186 is part of a preferred termination structure 91, which is described next in FIG. 3.

[0032] Termination structure 91 is formed on a periphery or perimeter of vertical FET structure 11. Structure 91 includes a termination region 159 that is formed at the same time as doped gate regions 59, and comprises the same conductivity type (e.g., p-type when structure 11 comprises an n-channel device). Termination structure 91 provides a means for controlling electric field spread and electric field shape during device

operation, and preferably is coupled to gate connecting region 79 as shown in FIG. 2.

5 **[0033]** By using multiple trench structure 28 according to the present invention, gate region 59 is placed deeper into channel regions 61 and is more separated from source regions 26 thereby improving gate blocking characteristics. Also, by using a doped gate region, the blocking characteristics are further improved compared to conventional Schottky gate designs. Also, because
10 structure 11 comprises a compound semiconductor material, structure 11 has a reduced gate charge, reduce gate resistance, and enhanced switching speeds compared to silicon based devices.

15 **[0034]** In addition, for a given output current and switching frequency, structure 11 dissipates less power thereby allowing one to use a smaller chip size and a reduced number of phases. Additionally, by using a reduced width second trench 34 and gate connecting regions 79 to couple a plurality of gate regions
20 together, the plurality of doped gate regions 59 are placed close together thereby improving device performance. Moreover, compound semiconductor structure 11 provides a preferred depletion mode or normally on FET device that has advantages for advanced multi-phase power
25 conversion applications because, among other things, a depletion mode device has a lower series resistance compared to an enhancement mode device.

30 **[0035]** Furthermore, structure 11 can handle more current per phase in a multiphase power conversion application compared to silicon-based or enhancement mode devices. For example, for a 120A/500 kHz application, three phases are required with structure 11 compared to four for a silicon-based device. For a 120A/1 MHz application, four phases are required with structure 11
35 compared to 5 for a silicon-based device. For a 120A/2 MHz application, four phases are sufficient using

structure 11 compared to seven for a silicon-based device. This also enables a smaller system size thereby saving on pc board space, which makes the structure according to the present invention a cost effective
5 alternative for high power/high frequency applications.

[0036] Vertical FET device 11 further provides a structure that enables an integration of an improved sense FET in a multi-chip configuration or a single chip configuration. FIG. 4 shows a circuit diagram of a main
10 vertical FET device or cells 41 and a vertical sense FET device or cells 42 according to the present invention. Main FET 41 and sense FET 42 includes source nodes 43 and 46 respectively. The FET devices share a common gate node 47 and a common drain node 48.

[0037] FIG. 5 is a top plan view of one embodiment of FIG. 4 showing a simplified chip layout 51. Gate pad 47 is coupled to main FET cells 41 through connecting region 53, and is coupled to sense FET cells 42 through
15 connecting region 49. Common drain 48 (not shown) is a backside contact in this embodiment. The desired current sensing ratio and accuracy is what determines the total area of sense FET cells 42 compared to the total area of main FET cells 41. The physical location of sense FET
20 device 42 on chip 51 is determined by electrical, thermal and package/board layout requirements. As shown, the source regions of sense FET 42 are electrically isolated from the source regions of main FET 41. Typically, the space requirements for sense FET 42 are less than main
25 FET 43, which provides a cost effective integration. Additionally, sense FET 42 preferably comprises a
30 depletion mode double trench compound semiconductor design.

[0038] FIG. 6 shows enlarged cross-sectional views of main FET 41 and sense FET 43 according to the present
35 invention. Main FET 41 and sense FET 42 can be separate devices or integrated as shown in FIG. 6. In this

embodiment, main FET 41 and sense FET 42 comprise a body of semiconductor material 613. Body of semiconductor material 613 preferably includes a starting substrate or wafer 614 and an epitaxial or drift layer 617 formed on wafer 614. Preferably, epitaxial layer 617 has a dopant concentration on the order of less than 5.0×10^{17} atoms/cm³, and a thickness greater than about 0.1 micron.

[0039] Main FET 41 further includes source regions 43, and sense FET 42 further includes source regions 46, which are formed, for example, in the same as source regions 26 in structure 11. Both FET devices include double gate structures 628, which are formed in the same way as gate structures 28. Both FET devices include doped gate regions 659, which are formed, for example, in the same way as doped regions 59. Sense FET source contact layer or layers 684 provide contact to sense FET source regions 46, and main FET source contact layer or layers 685 provide separate and electrically isolated contact to main FET source regions 43. Contact layer 688 provides a common drain contact for both main FET 41 and sense FET 42.

[0040] Thus it is apparent that there has been provided, in accordance with the present invention, a vertical compound semiconductor FET device. A trench within a trench gate structure provides a FET device with improved gate blocking characteristics. Additionally, the FET device has improved high frequency performance characteristics compared to conventional silicon FET devices including enhanced mobility, improved reverse recovery, lower on resistance, and reduced gate charging effects. In addition, the structure according to the present invention provides a sense FET structure that is integrated with a main vertical FET to provide current sensing for applications such as multi-phase power conversion. Furthermore, the structure according to the present invention provides an improved switching device

for high power/high frequency dc/dc power conversion applications compared to silicon-based switching devices and other enhancement mode switching mode devices.

[0041] Although the invention has been described and
5 illustrated with reference to specific embodiments thereof, it is not intended that the invention be limited to these illustrative embodiments. For example, the structure according to the present invention is suitable for p-channel structures. Those skilled in the art will
10 recognize that modifications and variations can be made without departing from the spirit of the invention. Therefore, it is intended that this invention encompass all such variations and modifications as fall within the scope of the appended claims.